Laboratori Nazionali di Frascati

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A WIDE BAND, D.C. COUPLED, FAST AMPLIFIER

M. COLI, S. LUPINI and V. SILVESTRINI

Laboratori Nazionali di Frascati del CNEN, Frascati, Roma

and

G. PENSO

Istituto di Fisica dell'Università di Roma and Istituto Nazionale di Fisica Nucleare, Sezione di Roma, Italy

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A very simple fast amplifier is described. The output pulse has a rise time of 2.5 ns with less than 15% overshoot and a gain of 10. The bandwidth of the amplifier extends up to 175 Mc/s and is flat up to 40 Mc/s. The gain is practically independent of temperature in the range from 10° C to 60° C. The amplifier is completely d.c. coupled and is therefore particularly suited for nuclear experiments with very high repetition rates.

1. Introduction

Fast amplifiers can be designed for two different purposes: radio frequency or pulse amplification.

R.f. amplifiers should have constant gain as a function of frequency, while pulse amplifiers should have a short rise time at the output, with an overshoot as small as possible[1]).

Pulse amplifiers are frequently used in nuclear experiments, either in front of a coincidence or in front of a pulse height analyzer.

In the first case the rise time at the output of the amplifier determines the lower limit of the coincidence resolving time. In the second case a very good short term and long term stability is needed. Fast rise time and good stability are frequently conflicting design requirements.

Two different techniques have been generally followed up to now in fast amplifiers design. The first one is the distributed amplification technique[2]), which played a prominent role with tube amplifiers. Since distributed amplifiers do not present a good gain stability, their interest for nuclear electronics is obsolete in spite of modern results*. The second one is the low level, high

* Recently systems have been developed for carried amplification, which is the modern trend for high output level and very fast rise time [3]).

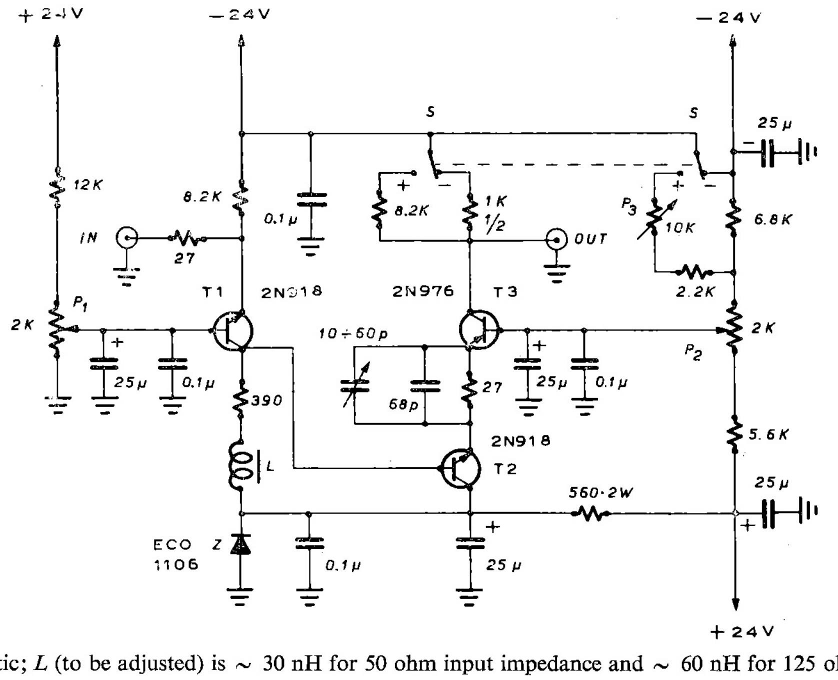

Fig. 1. Circuit schematic; L (to be adjusted) is ~ 30 nH for 50 ohm input impedance and ~ 60 nH for 125 ohm input impedance.

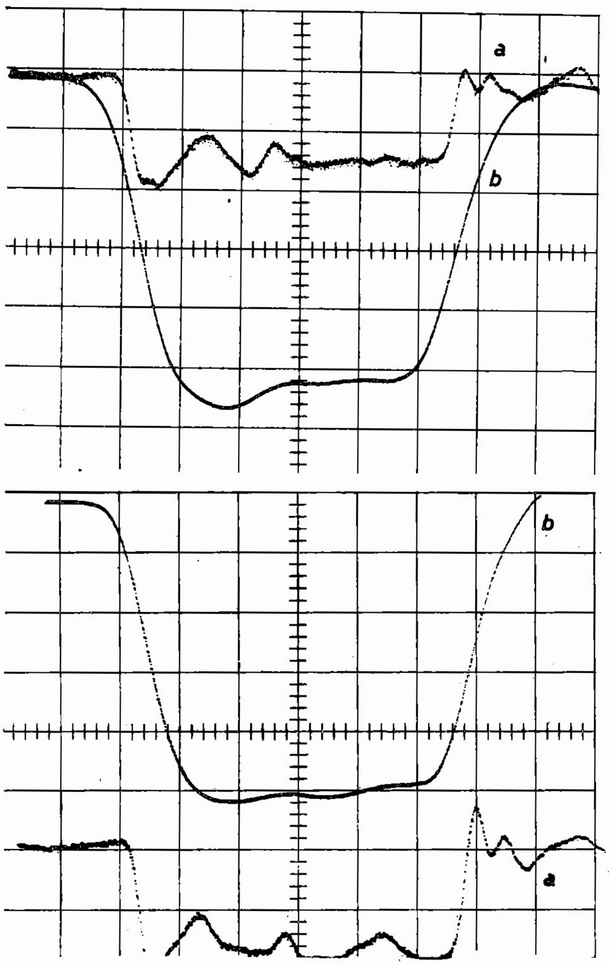

Fig. 2. Input and output pulses for different values of the peaking inductance L. Vert.: a) Input: 50 mV/cm, b) Output: 200 mV/cm; Hor.: 2 ns/cm.

speed technique allowed by modern semiconductors[4,5]).

Other techniques successfully used with tubes, have also been applied to semiconductor-amplifiers in recent years[6-9]).

The requirement of fast rise time and of a wide frequency band (down to some kc/s and up to a fraction of Gc/s) generally makes the circuitry of semiconductor-amplifiers rather complex[5,6]). The presence of many active components involves a lack of long term gain stability.

We have studied a fast amplifier with Gc/s transistors, whose simplicity and good performances give some important advantages.

2. The circuit

The circuit schematic is shown in fig. 1. The circuit consists of complementary transistors d.c. coupled from input to output (both at zero level) in grounded-base and grounded-collector connection only.

The power amplification functions are separated on different transistors. The input transistor T_1 (n-p-n type), grounded-base, provides voltage gain. Transistor T_2 (n-p-n type), a grounded-collector stage, provides current gain. Both transistors are thus connected to give the maximum gain-bandwidth product. The output transistor T_3 (p-n-p type) is also grounded-base connected, and transfers the signal to the output at zero level on its high collector impedance with a small contribution to the total gain (factor of 1.5 voltage gain). Compensation for collector capacitance is easily obtained by the peaking coil L ($\sim$ 60 nH, to be adjusted) on the collector of T_1. Sensitive control of the bandwidth is also obtained by a peaking capacitor across the resistor from the emitter of T_2 to the emitter of T_3.

The amplifier can work with either negative or positive input pulses. If we want identical performances for both polarities, the static current I in transistors T_2 and T_3 must be properly adjusted through the switch S (fig. 1).

For negative pulses, the output dynamics is determined by the current I: for S in the position $-$, I is set to $\sim$ 23 mA, to get a maximum dynamic current of 20 mA at the output.

With S in position $-$, the power dissipation limits V_{CE} of the 2N976 transistors to 4 V. This does not affect the overall bandwidth, also if its gain is as high as 2. The 2N918 emitter follower T_2 can easily handle a 23 mA current with $f_T \sim$ 500 Mc/s ($V_{CB} \geqq 3$ V).

For positive going pulses (S in position $+$), the current I is set to $\sim$ 3 mA. Also in this case, f_T is of the order of 500 Mc/s.

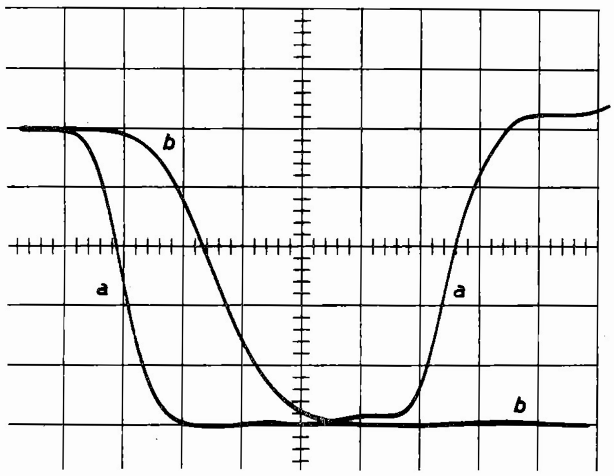

Fig. 3. Rise and fall time of the output pulse. Vert.: 200 mV/cm, Hor.: a) 2 ns/cm, b) 1 ns/cm.

A static current of 5 mA is recommended in the input transistor T_1, for an over-all current gain of 20 dB and pulses of either polarity.

The output is fed directly by the collector of T_3. Addition of a current amplifier at the output allows one to operate transistors T_2 and T_3 at a lower current level. A greater output current can be obtained in this way, but the rise time will deteriorate a little.

The voltage gain, rise time and delay time of the amplifier, have been calculated (see appendix) assuming for each transistor the equivalent circuit of fig. 8.

We have found:

Voltage gain $G = 11$
Rise time $T_R = 2 \div 3.5$ ns
Delay time $T_D = 3$ ns

These values are in fairly good agreement with the measured ones.

3. Operation and results

Input and output d.c. levels can be adjusted through potentiometers P_1 and P_2 (fig. 1). Proper adjustement of the potentiometer P_3 allows one to maintain a zero level at the output when the switch S is operated.

Ambient temperature excursion from 10° C to 60° C gives rise to a drift of the output d.c. level of ~ 20 mV, while the gain over the full bandwidth does not practically change (It changes certainly less than 1%).

The rise time deteriorates a little with increasing temperature: being ~ 2 ns at 10° C, it becomes ~ 3 ns at 50° C and 4 ns at 60° C. The delay time increases from 1.8 ns to 2.9 ns passing from 10° C to 50° C.

The impulsive tests of the circuit are shown in fig. 2, for different values of the peaking inductance coil on T_1. Test pulses were obtained from a mercury wetted pulse generator with a rise time of ~ 0.5 ns. The rise time at the output is always between 2 ns and 2.5 ns, with a voltage gain between 8 and 10 (fig. 3). The gain-rise time quotient for the amplifier is then about 4 ns^{-1}.

The bandwidth has been measured using a sampling oscilloscope Tektronix 661. The results, for different values of inductance L, are shown in fig. 4. With an overcompensation of ~ 15%, we easily obtain a cut-off frequency of 175 Mc/s.

The output wave forms for either polarity, are shown in fig. 5.

A linearity test has been done with the help of a 200 channels analyzer. The result is shown in fig. 6. The differential linearity* is better than 3%.

* Maximum percentage variation of the slope of the response curve (fig. 6), in operation region.

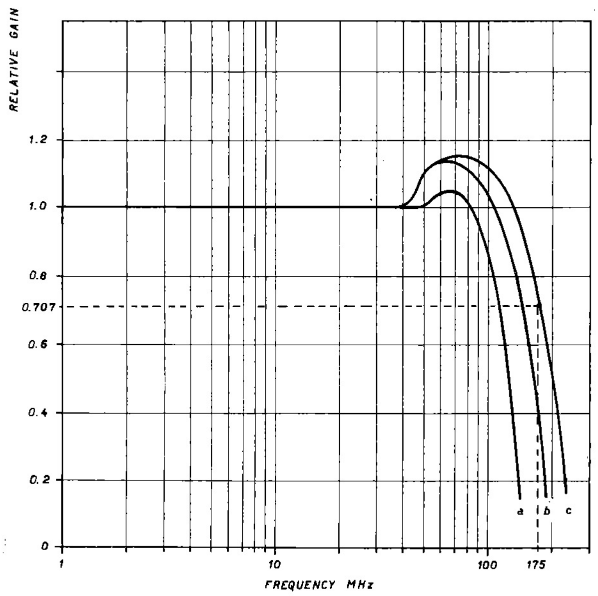

Fig. 4. Bandwidth of the amplifier. Curves a, b and c refer to increasing values of inductance L.

Modular assembly allows series cascading of amplifiers. A series of two amplifiers has been tested by us. We obtained a gain of 100 with 4.5 ns rise time. Impulsive output waveforms for this case are shown in fig. 7.

The ratio

$$R = \frac{\text{amplifier gain} - \text{bandwidth product}}{\text{transistor gain} - \text{bandwidth product}\ (f_T)} \text{ is } \sim 1.9$$

having taken as f_T the maximum value of 900 Mc/s. This value of R is a good technical achievement, considering the small number of transistors involved.

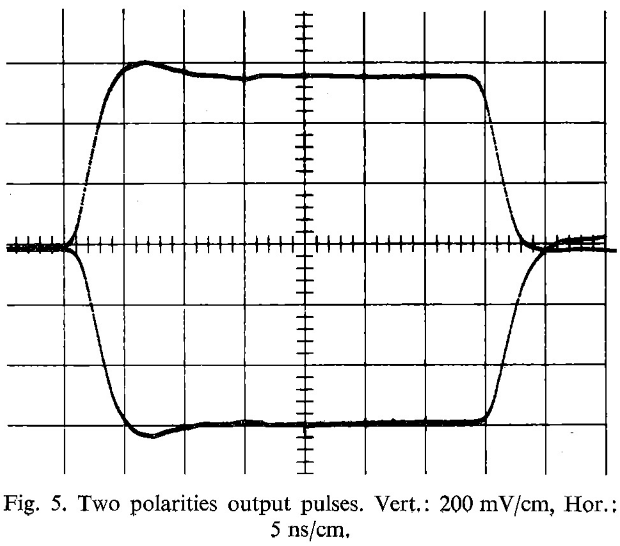

Fig. 5. Two polarities output pulses. Vert.: 200 mV/cm, Hor.: 5 ns/cm.

4. Conclusions

Although very simple in its design, the amplifier described has a frequency performance which is probably close to the best obtainable with the transistors involved.

The gain stability deriving from its simplicity, along with its flexibility, makes this circuit able to match the requirements of many nuclear experiments.

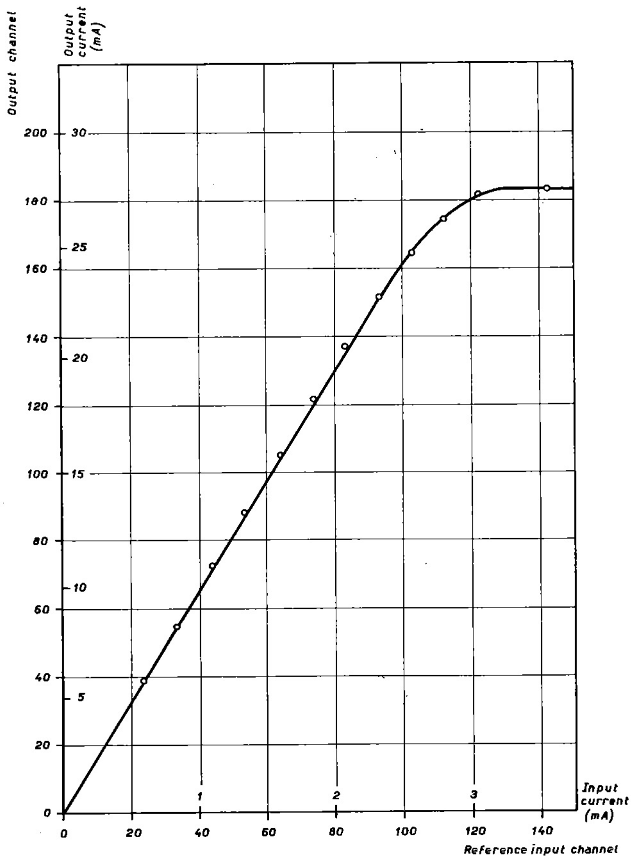

Fig. 6. Linearity test of the amplifier.

5. Characteristics

Input: Referred to ground at d.c. zero level
Signal polarity: either, according to the position of the switch S (fig. 1)
Signal dynamics: $\pm$ 2 mA
Input impedance: 50 ohm*

Output: Referred to ground at d.c. zero level
Signal polarity: same as input
Rise time $\simeq 2 \div 2.5$ ns (from 10% to 90% of max. amplitude)
Delay time $\simeq$ 0.7 ns (at 10% of max. amplitude)
$\simeq$ 1.8 ns (at 50% of max. amplitude)
Signal dynamics: $\pm$ 20 mA
Output impedance: $\sim$ 1 kΩ or $\sim$ 8.2 kΩ according to the position of switch S (fig. 1); the signal is fed directly into output cable (e.g. 50 ohm, 75 ohm or 125 ohm)

Current gain: 20 dB
Bandwidth: $0 \div 175$ Mc/s
Gain-rise time quotient: 4 ns^{-1}
Gain-bandwidth product: 1750 Mc/s.

* For an input impedance of 125 ohm, the input resistance must be changed into 82 ohm and the collector load of transistor T_1 must be 470 ohm.

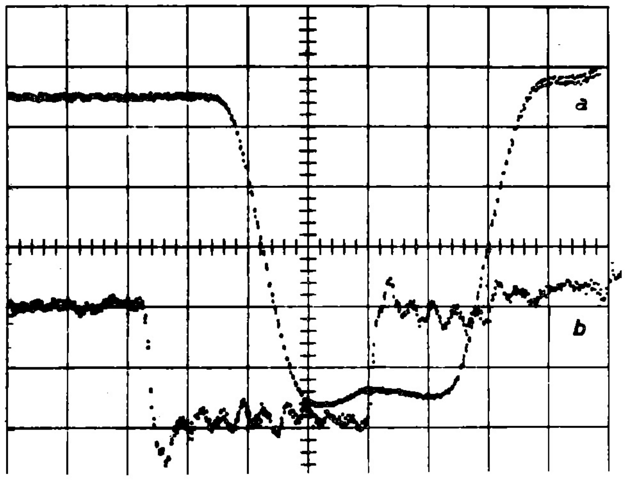

Fig. 7. Input and output pulses from two series amplifiers. Vert.: a) output: 200 mV/cm, b) input: 5 mV/cm; Hor.: 5 ns/cm.

Appendix

The gain, rise time and delay time of the amplifier have also been calculated; we report here some details about the calculations and their results.

In evaluating the rise time (T_R) and the delay time (T_D), we have used the definitions given by W. C.

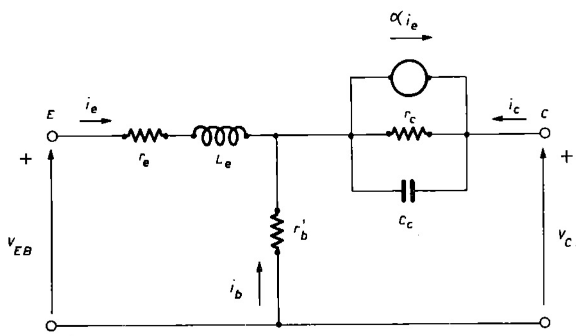

Fig. 8. Equivalent circuit used in computing rise time and delay time. $r_e = 15\,\Omega$; $r_c = 1\,\text{k}\Omega$; $r_b' = 10\,\Omega$; $L_e = 20\,\text{nH}$; $C_c = 1.5\,\text{pF}$.

Elmore[10]). Precisely, let $G(s)$ be the complex gain of the amplifier; if we are able to put $G(s)$ in the form:

$$G(s) = \frac{a_0}{b_0} \frac{1 + a_1 s + a_2 s^2 + \ldots + a_n s^n}{1 + b_1 s + b_2 s^2 + \ldots + b_m s^m}\,; \; m > n$$

then we have:

$$T_D = b_1 - a_1$$
$$T_R^2/2\pi = b_1^2 - a_1^2 + 2(a_2 - b_2).$$

To carry out the calculations, we have represented each transistor by the equivalent circuit of fig. 8. The values of r_c, C_c, r_b' are known from the data sheets, while L_e and r_e have been measured with a high frequency RX meter, in the frequency range from 50 to 150 Mc/s. We find $L_e \simeq 20$ nH, $r_e \simeq 15$ ohm.

The rise time and delay time depend critically on the value of the peaking inductance (L) and capacitor (C) (fig. 1) as already observed. For values of L in the range 50 ÷ 150 nH and values of C between 50 pF and 100 pF we have obtained an overall rise time varying between 2 ns and 3.5 ns and a delay time of about 3 ns.

The gain has also been evaluated, assuming for r_e and r_b' the low frequency values of 4 ohm and 30 ohm respectively. We obtain:

$$A = A_{CB1} \cdot A_{CC2} \cdot A_{CB3} = 11$$

where A_{CB1} and A_{CB3} are the gains of the common-base stages and A_{CC2} the gain of the common-collector stage.

In conclusion the calculated values of rise time, delay time and amplification are in fairly good agreement with the experimental ones.

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